5. RF Amplifier

Chapter 5 Goals

- Introduce the common source FET amplifier and perform LTspice simulation
- Add a CE amp; LTspice simulation
- Breadboard the RF amplifier circuit

An RF amplifier is needed to boost the weak AM signal received by the antenna prior to audio signal extraction by the detector. Our RF amplifier will consist of two stages as shown in Figure 5.1. The first stage is a common source (CS) amplifier based on the field effect transistor, or FET. The CS amp features high input impedance so most of the weak signal will appear across the input terminals, but suffers from a fairly small gain. To increase gain, the second stage is a common emitter (CE) amplifier as studied in Chapter 2.

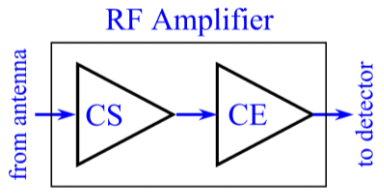


Figure 5.1: Two stage RF amplifier consists of a common source (CS) amplifier and common emitter (CE) amplifier.

5.1 The Common Source Amplifier

5.1a The FET

Figure 5.2 shows the circuit symbol for an n-channel junction field effect transistor. Operation of the n-channel JFET is similar to operation of the n-channel MOSFET (MOS stands for metal-oxide-semiconductor) that is one of the most heavily used devices constructed by the integrated circuit industry. We choose to use JFETs rather than MOSFETs because the JFET is not so static sensitive, and can therefore be used in a lab environment without special handling.

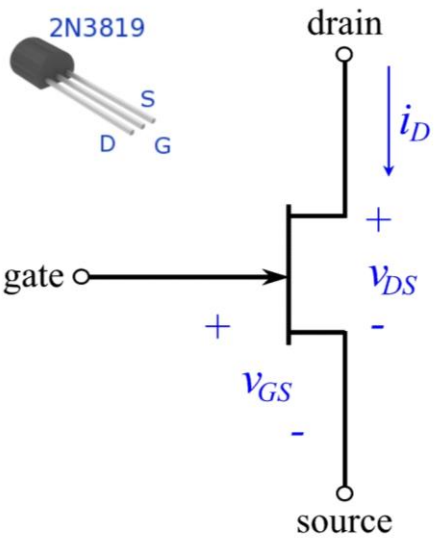


Figure 5.2: The field-effect transistor (FET)

A typical family of operating curves is shown in Figure 5.3. The FET has three main regions of operation called pinchoff, ohmic and saturation. The saturation region of a FET is analogous to the forward active region of a BJT, and is where we want to bias the device for operation in an amplifier. Saturation requires that

$$v_{DS} \geq v_{GS} - V_P$$
$$V_P \leq v_{GS} \leq 0$$

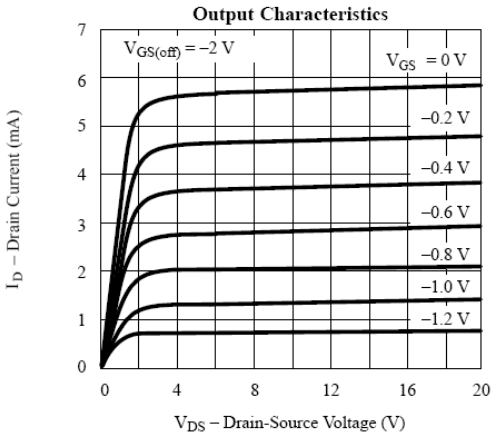


Figure 5.3: typical family of curves for a FET (http://www.tubecad.com/2007/09/blog0119.htm)

where V_p is the *pinchoff voltage*. For the simple model of FET operation, we then have

$$i_D = \frac{I_{DSS}}{V_p^2}\left(v_{GS} - V_p\right)^2 \qquad (1)$$

where I_{DSS} is the drain-to-source current saturation (also known as the *zero gate voltage saturation current*).

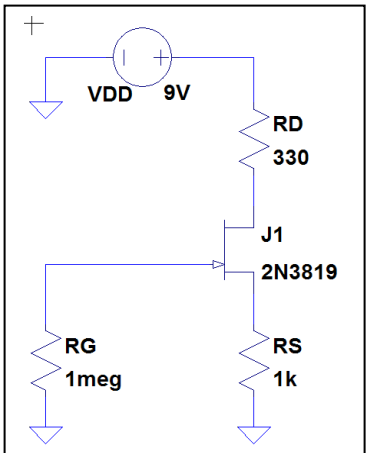


Figure 5.4: n-channel JFET in a DC biasing network used to establish the Q point.

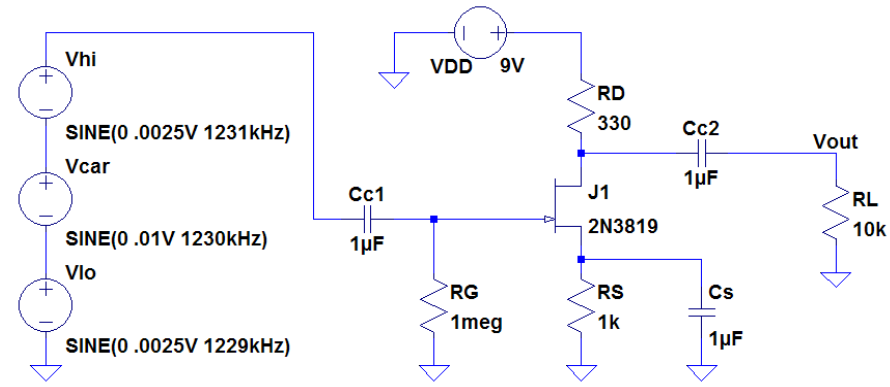


Figure 5.5: Common source (CS) amplifier with AM input

A simple DC biasing network is shown in Figure 5.4. For the DC analysis, the total drain current i_D in (1) replaced by the DC value I_D, and v_{DS} is replaced by V_{DS}. Note that the gate current (current through RG into the gate), is zero, so the DC voltage at the gate is 0V. The DC voltage from gate to source is then $V_{GS} = V_G - V_S = -V_S$. The voltage at the source is equal to $I_D R_S$ so,

$$V_{GS} = -I_D R_S \qquad (2)$$

Inserting (2) into (1) and expanding, we arrive at

$$I_D^2 + BI_D + C = 0$$

where

$$B = \left(\frac{2V_p}{R_S} - \frac{V_P^2}{R_S^2 I_{DSS}} \right), \quad C = \frac{V_P^2}{R_S^2}$$

The quadratic solution for I_D is then

$$I_D = \frac{-B \pm \sqrt{B^2 - 4C}}{2} \qquad (3)$$

where only one solution satisfies the requirements for saturation. Once I_D is found, then

$$V_{DS} = V_{DD} - I_D \left(R_D + R_S \right)$$

The Q-point is then (V_{DS}, I_D).

Exercise 5.1: The approximate parameter values for the J2N3819 are V_P = –3V and I_{DSS} = 10 mA. With the bias circuit values shown in Figure 5.4, determine the Q-point.

hand calculation: Q(_____, _____)

A common source amplifier is shown in Figure 5.5 Calculation of gain and input impedance for the CS amplifier requires a small signal AC model as shown in Figure 5.6(a). The JFET transconductance g_m depends on the biasing condition as

$$g_m = \frac{2I_{DSS}}{V_p^2}\left(V_{GS} - V_P\right) \qquad (4)$$

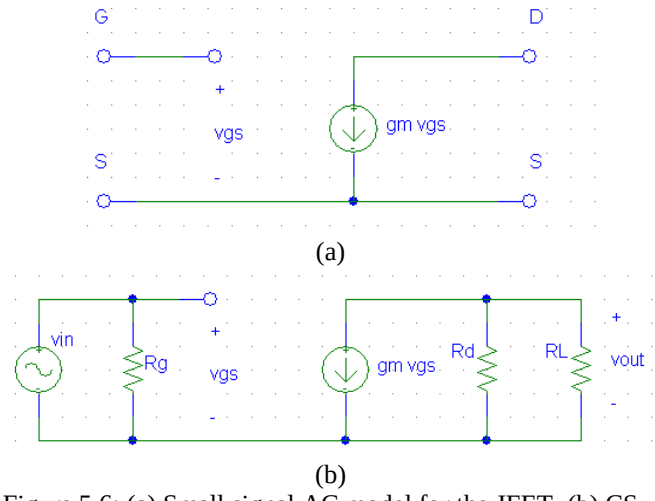


Figure 5.6: (a) Small signal AC model for the JFET, (b) CS amp model

Exercise 5.2: Calculate gm for the JFET of Exercise 5.1.

g_m = _____

Now we can draw the AC circuit model for the common-source amplifier, as shown in Figure 5.6(b). It is easy to see that the gain is

$$A = \frac{v_{out}}{v_{in}} = -g_m R_d \| R_L \qquad (5)$$

Exercise 5.3: Calculate gain for the CS amplifier of Exercise 5.1.

A = _____

Here we see that the gain of the CS amplifier is proportional to the resistance seen by the drain, which in this case is the parallel combination of 330 Ω and 10 k Ω. To increase gain, we can place an *RF Choke* (RFC) between the 330 Ω resistor and the drain, as shown in Figure 5.7. An ideal RFC will appear as an open circuit to the RF signal. An actual RFC should therefore have a very high impedance.

Exercise 5.4: At 1230 kHz, determine the impedance for:

(a) L = 1 μH Z = _____

(b) L = 1000 μH Z = _____

Exercise 5.5: Calculate gain for the CS amplifier of Exercise 5.1 if an ideal RFC is used between RD and the JFET drain.

A = _____

5.2 LTspice Simulation of CS Amplifier

1. Construct the circuit shown in Figure 5.4.

- To place the JFET, in "Select Component Symbol" choose the njf (n-channel JFET). Right click on the placed part, and press the "Pick New JFET: button. Then, select the 2N3819.

2. Run a DC Operating Point and determine the transistor Q-point.

LTspice calculation: Q(_____, _____)

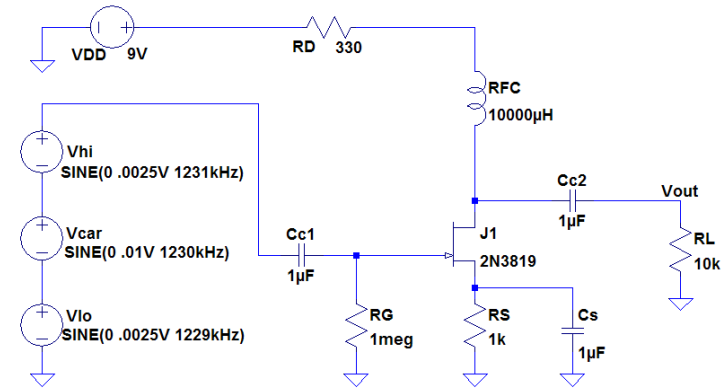


Figure 5.7: CS amplifier after adding an RFC.

3. To the JFET circuit of Figure 5.4 we add the coupling and bypass capacitors, AM source (Vhi, Vcar, and Vlo sinusoidal sources), and load resistance to build a CS amplifier as shown in Figure 5.5. Build this circuit in LTspice.

4. Perform a 'transient analysis' with the Stop Time set to 4 ms. Run the simulation. Determine gain by first setting a voltage marker at the input (left of Cc1) and reading the input peak to peak signal:

Vin(pk-pk)=_____

Now set a voltage marker at the output (right of Cc2) and reading the output peak to peak signal:

Vout(pk-pk)=_____

Evaluate the gain:

Gain = Vout/Vin = _____

Comment on this result:

5. Add the RFC to your CS amplifier as shown in Figure 5.7. Resimulate and find the gain.

Vin(pk-pk)=_____

Vout(pk-pk)=_____

Gain = Vout/Vin = _____

6. With R_D out of the picture as far as gain is concerned, we can now study the gain as a function of load resistance. Modify the load resistance in Figure 5.7 to re-simulate and find the gain (in dB) for different load resistances. Fill in Table 5.1. Plot gain (dB) versus load resistance in Figure 5.8.

Table 5.1: calculating gain vs load resistance for Figure 5.7, given

Gain (V/V) = Vout(pk-pk)/Vin(pk-pk)

Gain (dB) = 20*log(Gain(V/V)), Vin(pk-pk) = _____

R_L	Vout(pk-pk)	Gain (V/V)	Gain (dB)
1 MΩ			
100 kΩ			
10 kΩ			
1 kΩ			
100 Ω			

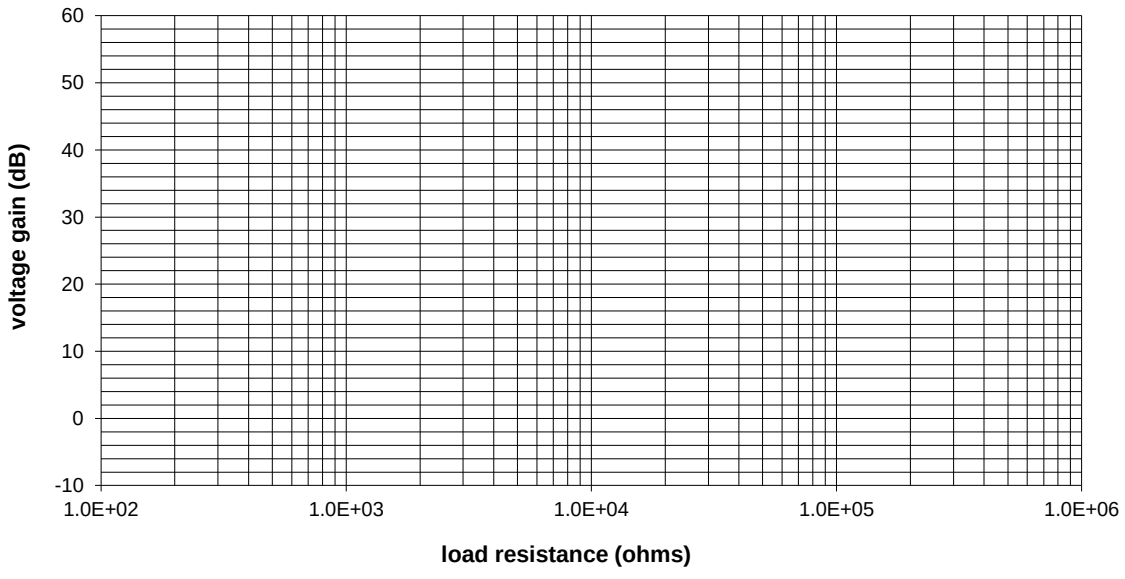


Figure 5.8: Blank chart for filling in Table 5.1 data

5.3 LTspice Simulation: Adding a CE amp to the CS amp

To get more gain out of our RF amp, we can add a CE amp to the output of the CS amp.

1. Assemble the circuit shown in Figure 5.9.
- In the construction phase of this chapter, the three signal sources, Vhi, Vcar and Vlo, will be realized using the AM output of your BK Precision 4040 generator with carrier set to ~1230 kHz and 1 kHz internal modulation. The amplitudes are chosen to achieve ~50% modulation in the simulation.

2. Simulate with a 4ms stop time as before. Determine G(V/V), the gain in V/V. Also calculate G(dB), the gain in dB (G(dB) = 20*log(G(V/V)). Enter these results in Table 5.2 for R_L = 1 MΩ.

3. If you place a voltage marker on the drain of J1, you can calculate the gain of just the CS amplifier. Based on this gain and your plot of Figure 5.8, what do you estimate is the impedance seen by the CS amp looking into the input of the CE amp?

Table 5.2: calculating gain vs load resistance for the two-stage RF amp of Figure 5.8

R_L	Vout*	G (V/V)	G (dB)
1 MΩ			
100 kΩ			
10 kΩ			
1 kΩ			
100 Ω			

*you can use amplitude or peak-to-peak values as long as you are consistent.

4. Change R_L, re-simulate, and fill in the rest of Table 5.2.

5. Superimpose the Table 5.2 data on Figure 5.8 using a different color or line style. Label your lines.

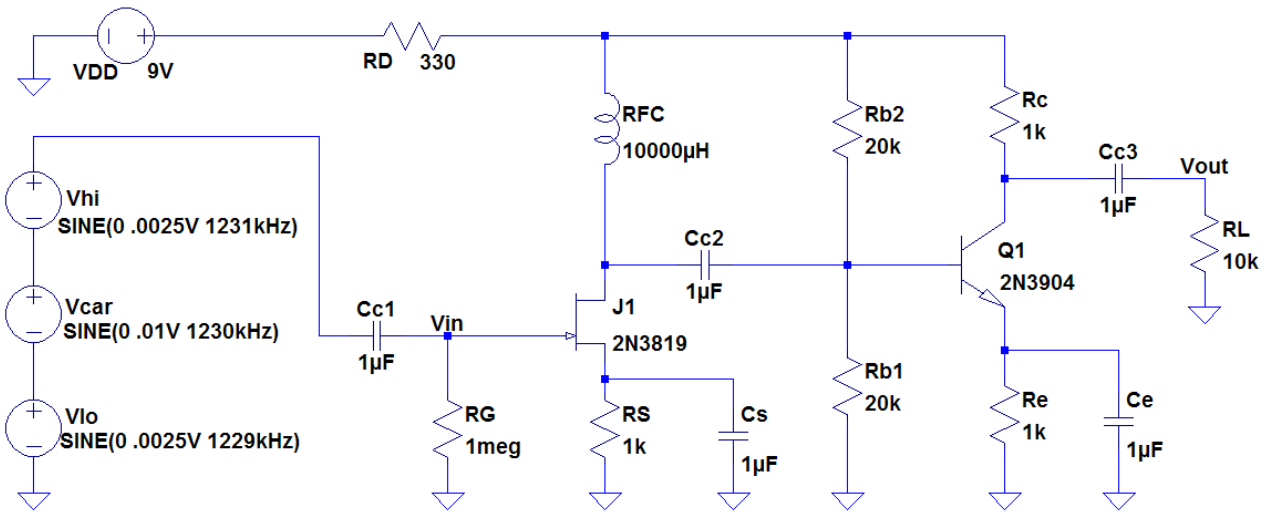


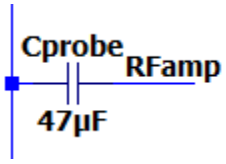
Figure 5.9: Two stage RF amplifier (CS amp + CE amp)

5.4 LTSpice Simulation: Full AM Radio

Since the goal of the lab is to build a fully functional radio, lets simulate a full radio! This will be valuable to you when you are troubleshooting in lab

1. Pick your favorite audio amplifier and favorite AM detector. **Comment** on your selection and explain why you are choosing these components.
2. Connect up your radio as follows: *RF amplifier* to *AM detector* to *audio amplifier*, and end the schematic with a 10Ω load resistance. Your schematic should be similar to Figure 5.12 (**but with your components of choice**). If you are choosing to use the LM386 audio amplifier, then substitute a different amplifier (such as the CE-CC) in your simulation.
   a. **Helpful Hint**: Make your schematic neat and easy to read as you will be building your circuit in lab.
3. Input an AM wave to your RF amplifier. Use the same set-up as in Figure 5.9, but divide the magnitudes of all three SINE inputs by 10. You can further reduce as needed.
4. Set the simulation to start at 10 seconds and end at 13 seconds. (This will give the circuit time to settle out). You can do this by right clicking your simulation command and modifying the times. It should look similar to:

   .tran 0 13ms 10ms .01ms
5. Plot the input of your system. Now plot the input of your system with the output of your RF amplifier on the same plot. The output should go through a filter cap. See hint below. **Comment on the results.**
   a. **IMPORTANT Hint:** When measuring nodes in circuit (such as the node between your RF amp and detector and the node between the detector and audio amp) you will need to set up a DC blocking capacitor to take this measurement accurately. Add a 47 µF capacitor to the measurement point where one side connects to the point of interest, and the other end is floating. On this floating node place your node label for plotting. Similar to below:



   b. **Helpful Hint**: Label all measurement points (nodes)
   c. **Helpful Hint 2**: Tweak component values if needed to improve performance. **This is your radio!**
6. Plot the input to your AM detector and the output of the AM detector on the same graph. Both of these measurements need to be through DC filter caps. Shift up the output of detector so it is visible. **Comment on the results.**
7. Plot the input of your audio amplifier (probe after DC filter cap) and the output of your audio amplifier on the same plot. **Comment on the results.**
8. FINALLY, plot the input to your radio and the output at the 10Ω load! **Comment on the results and what you think of your selected radio.**
9. Tweak the AM wave power to your radio and see what happens. I would recommend a few simulations with larger and smaller power levels if possible so you can get a better feel for your radio.

5.5 RF Amplifier construction

1. Construct the Common Source amplifier shown in Figure 5.5 with R_L = 10 kΩ. Measure and record the Q point and the gain in Table 5.3. Repeat for R_L = 1 kΩ and R_L = 1 MΩ.

2. Now add the RFC, as in Figure 5.7. Record the new gain for the three values of R_L in Table 5.3.

3. Add the common emitter amplifier (Figure 5.9). Record the Q point for the npn BJT.

   Q(npn BJT) = (_____. _____)

4. Measure the gain with various values of load resistance and fill in Table 5.4. Plot this data in Figure 5.10.

5. Now connect the output of the RF amplifier to the input of your detector (see Figure 5.12).

6. Test your radio with an appropriate input signal. The next step (Chapter 6) will be to add an antenna.

Table 5.3: Measurements on CS amp

	R_L=1MΩ	R_L=10kΩ	R_L=1kΩ
Q(VDS,ID)			
G (V/V) (no RFC)			
G (V/V) (with RFC)			

Table 5.4: Gain of two-stage amp

RL	Gain (V/V)	Gain(dB)
1 MΩ		
100 kΩ		
10 kΩ		
1 kΩ		
100 Ω		

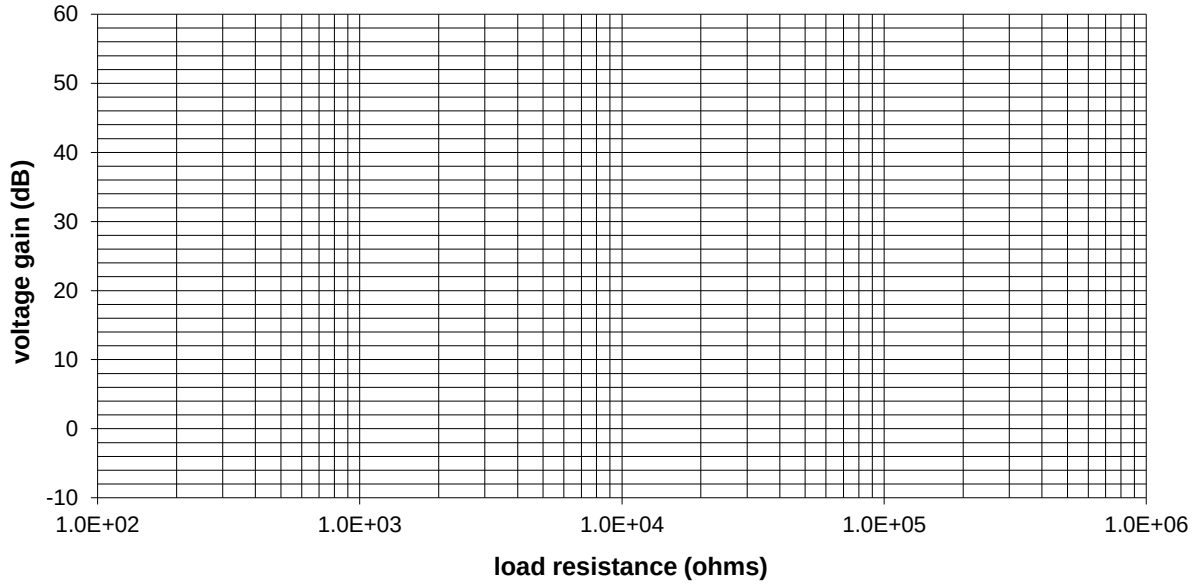


Figure 5.10: Blank chart for filling in Table 5.4 data

Note 1: This might be a good time to carefully and neatly rewire your AM radio (for instance, see Figure 5.11). Try to minimize lead and wire lengths, but don't cut the leads too short to fit into the breadboard. It is a good idea to build and test each block at a time as you do the re-assembly.

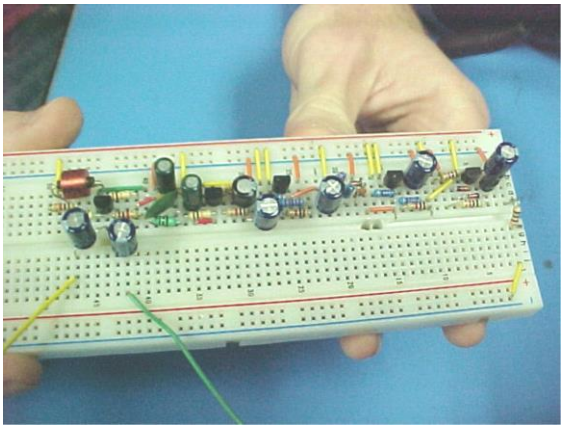


Figure 5.11: neatly breadboarded circuit

Note 2: The signal coming from the antenna will be very weak. Some students have improved radio performance by adding a common collector stage (see Figure 3.1) between the common source and common emitter stages. The high input impedance of the CC stage results in significantly higher gain for the CS stage (see Figure 5.8).

One caveat is that LTspice simulation of the CS-CC-CE RF amp will show a lot of distortion unless the input signal level is lowered by an order of magnitude or so. However, the VSIN component may not allow you to enter voltage levels this low. In this case, a resistive divider (90 kΩ in series with the sources and 10 kΩ to ground) will give an order of magnitude decrease in the signal entering the RF amplifier.

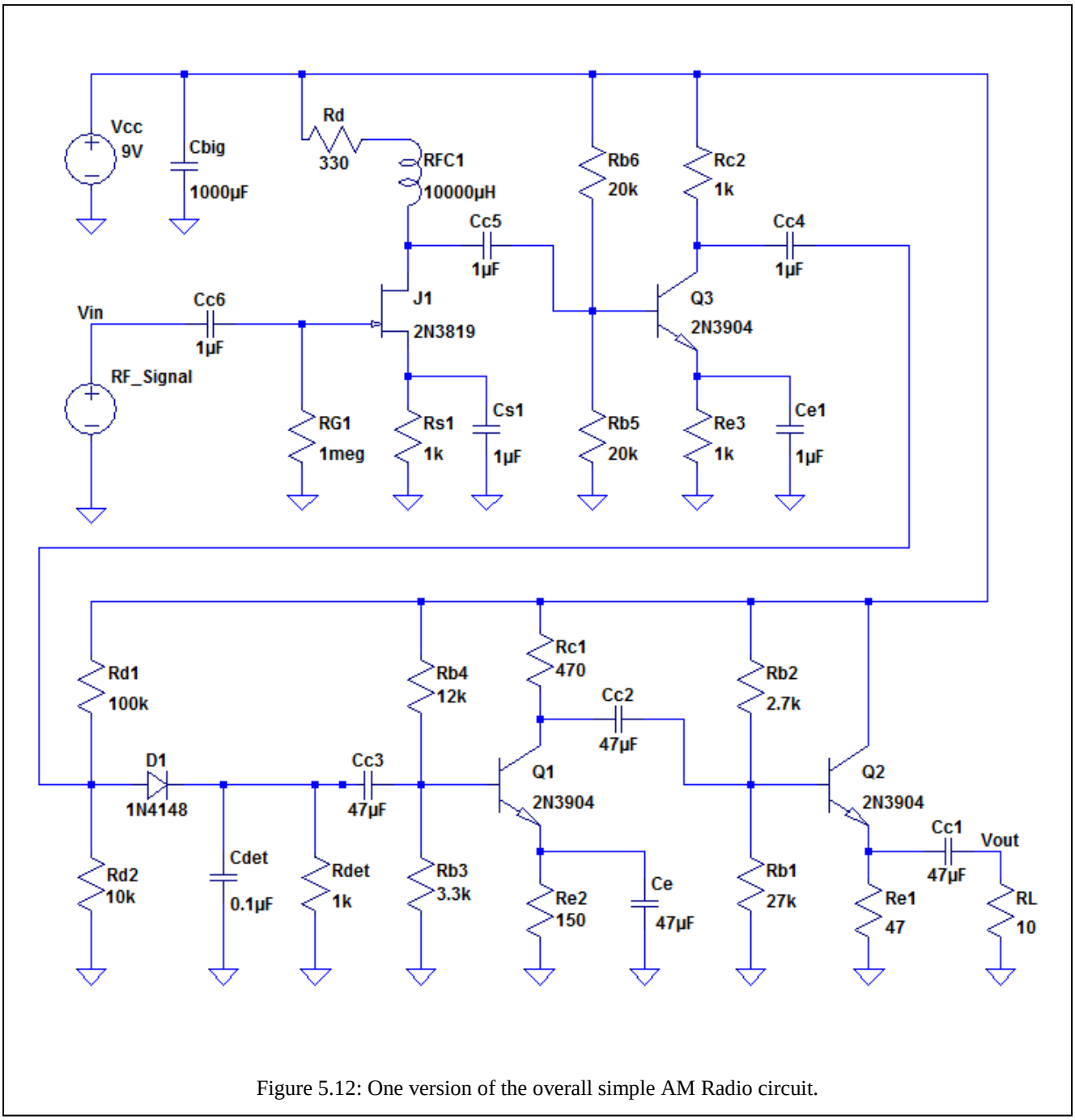


Figure 5.12: One version of the overall simple AM Radio circuit.